What is claimed is:

1. A memory apparatus comprising:

a rewritable nonvolatile memory; and

a control circuit,

wherein the memory apparatus brings logical addresses into correspondence with physical addresses of the nonvolatile memory and retains a piece of number-of-rewrites information for each logical address,

wherein the control circuit can perform a replacement process of a piece of memory information on the nonvolatile memory, and

wherein the replacement process is a process of replacing a first physical address corresponding to a given logical address judged to have a small number of rewrites based on the pieces of number-of-rewrites information with a second physical address so as to bring the given logical address into another correspondence with the second physical address and performing data transfer according to the replacement.

2. The memory apparatus of Claim 1, wherein the second physical address is a free physical address used for a correspondence with no logical address.

3. The memory apparatus of Claim 1, wherein the second physical address is a physical address corresponding to a second logical address of the logical addresses, having a larger number of rewrites in comparison to the given logical address having

the small number of rewrites, and

wherein the second logical address is changed so as to be brought into correspondence with the first physical address to which the given logical address having the small number of rewrites was assigned.

4. The memory apparatus of Claim 1, wherein the replacement process can be performed concurrently with a process in response to a direction for writing provided from an outside of a memory card.

5. The memory apparatus of Claim 4, wherein the replacement process can be performed when the number of rewrites of the logical address targeted for the process in response to the direction for writing reaches a given number of times.

6. The memory apparatus of Claim 5, wherein the replacement process can be performed on a logical address having a smallest number of rewrites, of arbitrarily extracted logical addresses.

7. The memory apparatus of Claim 4, wherein during the process in response to the direction for writing, the control circuit brings the logical address targeted for the process into correspondence with a third physical address and performs data rewrite.

8. The memory apparatus of Claim 7, wherein the nonvolatile memory has an address translation table in which correspondences of the logical addresses and physical addresses

are defined.

9. The memory apparatus of Claim 8, wherein the number-of-rewrites information for each logical address is retained in a region of the physical address corresponding to the logical address.

10. The memory apparatus of Claim 8, wherein the number-of-rewrites information for each logical address is retained in a number-of-rewrites table.

11 A memory card comprising:

a rewritable nonvolatile memory; and

a control circuit,

wherein the memory card brings logical addresses into correspondence with physical addresses of the nonvolatile memory, and retains a piece of number-of-rewrites information for each logical address,

wherein the control circuit can executes a rewrite process of the nonvolatile memory in response to a direction for writing from an outside, and a replacement process of memory information on the nonvolatile memory, and

wherein the replacement process is a process of replacing a first physical address corresponding to a given logical address judged to have a small number of rewrites based on the pieces of number-of-rewrites information with a second physical address so as to bring the given logical address into another correspondence with the second physical address and performing

data transfer according to the replacement.

12. A controller, performing host interface control and memory control on a rewritable nonvolatile memory,

wherein the memory control includes control of bringing logical addresses into correspondence with physical addresses of the nonvolatile memory to manage a piece of number-of-rewrites information for each logical address, and control of a replacement process that can be executed in performing rewrite on the nonvolatile memory, and

wherein the replacement process is a process of replacing a first physical address corresponding to a given logical address judged to have a small number of rewrites based on the pieces of number-of-rewrites information with a second physical address so as to bring the given logical address into another correspondence with the second physical address and performing data transfer according to the replacement.

13. The controller of Claim 12, wherein the second physical address is a free physical address used for correspondence with no logical address.

14. The controller of Claim 13, wherein the second physical address is a physical address corresponding to a second logical address of the logical addresses, having a larger number of rewrites in comparison to the given logical address having the small number of rewrites, and

wherein the second logical address is changed so as to

be brought into correspondence with the first physical address to which the given logical address having the small number of rewrites was assigned.

15. The controller of Claim 12, wherein the replacement process can be performed concurrently with a process in response to a direction for writing on a volatile memory provided from an outside thereof.

16. The controller of Claim 15, wherein the replacement process can be performed when the number of rewrites of the logical address targeted for the process in response to the direction for writing reaches a given number of times.

17. The controller of Claim 16, wherein the replacement process can be performed on a logical address having a smallest number of rewrites, of arbitrarily extracted logical addresses.